TL-SBC 6620

Single Board Computer

User's Manual

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Chapter-1

General Information

The TL-SBC 6620 is a bus-100MHz Intel® BX chipset design PICMG bus Pentium®II-III-Celeron™ Industrial Single Board (I.S.B.) CPU card with features combine together to make it an ideal all-in-one industrial single board computer, enhanced I/O effects with VGA interface supports LCD Display panel and CRT Monitor on-board.

The TL-SBC 6620 also provides one set of PC/104 bus for 8/16-bit industrial application with based on PC/104 standard bus.

With onboard DMA33 of mode 4 to IDE drive interface architecture, the TL-SBC 6620 supports with maximum 33.3 MB/sec in data transfer rating to 4 pieces IDE drive connection. Design with Intel® 82443BX and 82371EB core logic chipset, the TL-SBC 6620 supports all series Pentium®II-III-Celeron™ operating at 233 ~ 650MHz. The on-board C&T® 69000 VGA chipset supports up to 1280 x 1024 256 colors display resolution with on-chip 2MBytes memory, and it provides both VGA CRT Monitor and LCD Panel display connection.

The advanced PICMG bus add-on connection of TL-SBC 6620 allows user could easily obtain both ISA's 16-bit and PCI's 32-bit full set signals from a full size PICMG slot for suitable plug into system with 8/16/32-bit ISA and-or PCI slots operating. The TL-SBC 6620 provides with two pieces 168-pin DIMM sockets support up to 1.0GBytes of main system memory.

A single Flash chip holds the system BIOS, and you can easy update the Flash BIOS by the Utility Update. Advanced USB and IR ports also provide for faster and easily in data transmission. You can also use the DOS version of the "DiskOnChip™" socket by issuing commands from the DOS prompt without the necessity of other software supports up to 144MB.

If a non-expect program cause halts, the onboard WDT Watch-Dog Timer will automatically reset the CPU or generate an interrupt. The watchdog is designed with hardware only and doesn't need any arithmetical functions of a real-time clock chip. This ensures the reliability in an unmanned or standalone system.

1.1 Major Features

- ✓ One axial-horizontal type Slot-1 socket at face-side for Intel® Pentium®II-III-Celeron™ 233～650 MHz Processors.
- ✓ Intel® 82443 BX chipset.
- ✓ PICMG add-on bus with on-board PC/104 bus connector for 8/16-bit supported.
- ✓ Two pieces DIMM sockets supports DRAM up to 1.0 GB.
- ✓ Two fast PCI DMA33-IDE connector support four IDE drives include large size hard disks, CD-ROM, tape backup etc.
- ✓ PnP I/O address & IRQ selection.
- ✓ Two high-speed RS-232 serial ports support 16C550 UART with 16-byte FIFO. One port provides RS-422/485 selection.
- ✓ One enhanced bi-directional parallel port, supports SPP/EPP/ECP.
- ✓ On board PS/2 Keyboard and PS/2 Mouse connector.
- ✓ On board W83977 super I/O.
- ✓ On-board C&T® 69000 SVGA adapter with on-chip 2MBytes memory supports VGA LCD Panel and CRT Monitor display.
- ✓ On board Intel® 82558 100-Based Network.
- ✓ "DiskOnChip™" Socket supported memory size up to 72 MB.
- ✓ On-board two USB ports and one IrDA port.
- ✓ Build-in one industrial WDT Watch-Dog-Timer.
- ✓ AWARD Y2K PnP Flash BIOS.
- ✓ Hardware Temperature Alarm

*It will be a Warning "beep" come out if the CPU's temperature reached 60℃. And it will stop as the CPU's temperature going down below 60℃ again.

1.2 Specifications

- **CPU:** One piece Intel® Pentium®II-III-Celeron™ 233/ 266/ 300/ 333/ 400/450/500/650MHz.
- **Bus interface:** PICMG bus, comply with ISA and PCI slot One on-board PC/104 bus connector.
- **Chipset:** Intel® 82443 BX bus-100MHz chipset.
- **Data bus:** 64-bit
- **Processing ability:** 64-bit
- **C&T VGA Controller:** C&T® 69000 VGA, on-chip 2 MB memory included, supports up to 1280x1024 256 colors VGA modes resolution. Also provides one 50-pin LCD Panel connector, one internal 10-pin VGA-CRT connector.
- **PCI Enhanced IDE Interfaces:** Total four IDE drives supports with Mode 3 & 4 DMA33 function provides transfer rate up to 33.3MB/sec.
- **RAM memory:** Two pieces 168-pin DIMM sockets supports up to 1.0 GBytes.
- **Cache memory:** Slot-1 socket supports Intel's Pentium®II-III-Celeron™ CPU with build-in 512KB Pipeline burst cache memory.
- **Floppy disk drive interface:** Supports up to two floppy disk drives.
- **LAN:** Intel 82558 supports 100-Based.
- **Parallel port:** Supports SPP/ECP/EPP.
- **Serial ports:** Two RS-232 ports with 16-byte FIFO 16C550 UART. One port provides RS-422/485 selection.
- **BIOS:** AWARD Y2K PnP Flash BIOS.
- **WDT Watchdog timer:** Periods set 1, 2, 10, 20 , 110 or 220 seconds, activity trigger with Reset or NMI.
- **DMA channels:** 7

- **Temperature Alarm:** Hardware monitoring.
- **Interrupt levels:** 15
- **Keyboard:** 6-pin mini-DIN connector or 5-pin header.
- **Mouse:** 6-pin mini-DIN connector support PS/2 type mouse.
- **USB:** Supports 2 USB header.
- **IR interface:** Supports one IrDA TX/RX header.
- **Flash memory Disk:** Socket for DiskOnChip™ (DOC).
- **Fuse:** Automatically resumes polyswitch resettable fuse.
- **Extra Power:** Provides one 4-PIN extra DC +5V/+12V power connector.
- **CMOS:** DS12B887 or equivalent device.
- **Power voltage requested:** +5V, +12V and -12V.
- **Maximum Power Consumption:** +5V@5A(350MHz PII), +12V@20mA,

  -12V@20mA.
- **Operating temperature:** 0-55°C (CPU need cooler).
- **Board size:** 7.3"(L) x 4.8" (W) (185mm x 122mm).

1.3 Delivery Package

The delivery package of TL-SBC 6620 includes all following items:

- ✲ One TL-SBC 6620 Industrial Single Board
- ✲ One Printer Port Bracketed Flat Cable
- ✲ One COM Port Bracketed Flat Cable
- ✲ Two IDE port Flat Cable
- ✲ One FDD port Flat Cable
- ✲ One PS/2 to Standard DIN type Keyboard Transfer Cable
- ✲ Utility Diskette
- ✲ User's Manual
- ✲ 5 pin ATX Power Connector Cable

Please contact with your dealer if any of these items are missing or damaged when purchasing. And please keep all parts of the delivery package with packing materials in case of you want to ship or store the product in feature.

Chapter-2

Hardware Installation

This chapter provides the information on how to install the hardware of TL-SBC 6620. At first, please follow up sections 1.3, 2.1 and 2.2 in check the delivery package and carefully unpacking. Following after, the jumpers setting of switch, watchdog timer and the DiskOnChip™ address selection etc.

2.1 Caution of Static Electricity

The TL-SBC 6620 has been well package with an anti-static bag in protect its sensitive computer components and circuitry from the damage of static electric discharge.

Note: DO NOT TOUCH THE BOARD OR ANY OTHER SENSITIVE COMPONENTS WITHOUT ALL NECESSARY ANTI-STATIC PROTECTION.

You should follow the steps as following to protect the board in against the static electric discharge whenever you handle the board:

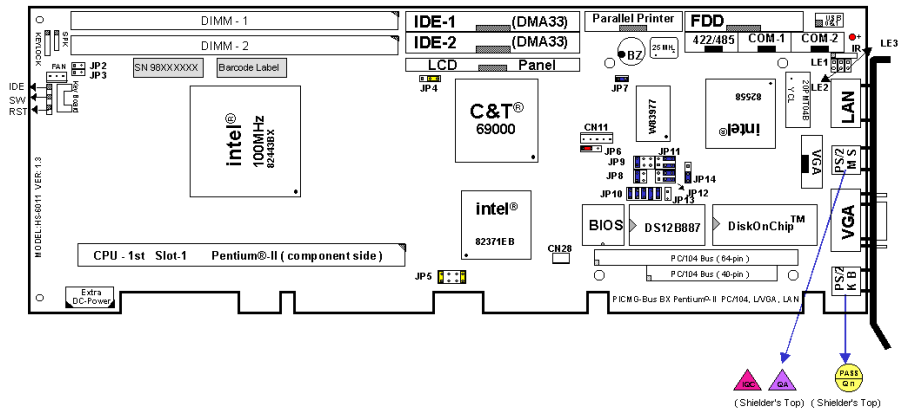
1. Please use a grounding wrist strap on whoever needs to handle the TL-SBC 6620. Well clip the ALLIGATOR clip of the strap to the end of the shielded wire lead from a grounded object. Please put on and connect the strap before handle the TL-SBC 6620 for harmlessly discharge any static electricity through the strap.
2. Please use anti-static pad for put any components or parts or tools on the pad whenever you work on them outside the computer. You may also in use the anti-static bag instead the pad. Please ask from your local supplier in help up your necessary parts on anti-static requirement.

2.2 Caution on Unpacking and Before Installation

First of all, please follow with all necessary steps of section 2.1 in protection the TL-SBC 6620 from electricity discharge. With refer to section 1.3, please check the delivery package again with following steps:

1. Unpacking the TL-SBC 6620, keep well storage of all packing material, manual and diskette etc. if has.
2. Is there any components lose or drop from the board? DO NOT INSTALL IF HAPPENED.
3. Is there any visual damaged of the board? DO NOT INSTALL IF HAPPENED.
4. Well check from your optional parts (i.e. CPU, SRAM, DRAM, ROM-Disk etc.) for completed setting all necessary jumpers setting to jumper pin-set and CMOS setup correctly. Please also reference to all information of jumpers setting in this manual.
5. Well check from your external devices (i.e. Add-On-Card, Driver Type etc.) for completed add-in or connection and CMOS setup correctly. Please also reference to all information of connector connection in this manual.
6. Please keep all necessary manual and diskette in a good condition for your necessary re-installation if you change your Operating System or whatever needs.

2.3 TL-SBC 6620's Layout



TL-SBC 6620's Layout

2.4 Quick Listing of Jumpers

JP2 (1-2 OFF) — Bus-Clock 66/100MHz Select
JP3 (1-2 OFF) — Manufacturer's Default Setting
JP4 (2-3 ON) — LCD 3.3/5.0V Power Select
JP5 (1-2, 7-8 ON) — Frequency Multiplier Select
JP6 (1-2 ON) — AT/ATX Power Select
JP7 (1-2 OFF) — Temperature Alarm
JP8 (1-2 ON) — RS-232/422/485 Select
JP9 (1-2 ON) — RS-232/422/485 Select
JP10 (1-2, 3-4 ON) — DiskOnChip™ Address setting
JP10 (5-6, 7-8, 9-10 ON) —WDT Time Scaling Select
JP11 (3-5, 4-6 ON) — RS-232/422/485 Select
JP12 (3-5, 4-6 ON) — RS-232/422/485 Select
JP14 (2-3 ON) — WDT Activity Select

2.5 Quick Listing of Connectors

JP1: RESET PIN

BZ1: ON-BOARD BUZZER
D4: ON-BOARD POWER-ON LED INDICATOR
D1, D2, D3: INTERNAL LAN'S LED INDICATORS
CN1: KEYLOCK CONNECTOR
CN2: SPEAKER CONNECTOR
CN3: HDD LED CONNECTOR
CN4: INTERNAL FAN'S POWER CONNECTOR FOR CPU
CN5: ATX POWER ON/OFF SWITCH
CN6: INTERNAL 5-PIN KEYBOARD CONNECTOR
CN7: POWER 4-PIN CONNECTOR
CN8: 1st IDE CONNECTOR
CN9: 2nd IDE CONNECTOR
CN10: INTERNAL VGA LCD CONNECTOR (HEADER 25x2)
CN11: ATX POWER CONTROL
CN12: PARALLEL PORT CONNECTOR
CN13: INTERNAL COM-2 RS-422/485 CONNECTOR (HEADER 5X2)
CN14: PC104-BUS 64-PIN ISA 8-BIT
CN15: PC104-BUS 40-PIN ISA 16-BIT
CN16: FDD CONNECTOR
CN17: INTERNAL COM-1 RS-232 CONNECTOR (HEADER 5X2)
CN18: INTERNAL COM-2 RS-232 CONNECTOR (HEADER 5X2)
CN19: INTERNAL VGA MONITOR CONNECTOR (HEADER 5X2)
CN20: USB PORTS CONNECTOR
CN21: IR CONNECTOR (6-PIN)
CN22: RJ-45 10/100-BASED LAN CONNECTOR
CN23: EXTERNAL COM-1 RS-232 CONNECTOR (DB9)
CN24: EXTERNAL MINI-DIN PS/2 MOUSE CONNECTOR
CN25: EXTERNAL VGA CONNECTOR (DB15)
CN26: EXTERNAL COM-2 RS-232 CONNECTOR (DB9)
CN27: EXTERNAL MINI-DIN PS/2 KEYBOARD CONNECTOR
DM1: DIMM SOCKET 0
DM2: DIMM SOCKET 1
SLOT-1: PEMTIUM™-II-III-Celeron™ PROCESSOR'S SOCKET
U24: DiskOnChip™ SOCKET
LE1~LE3: LAN LED CONNECTOR

2.6 Jumper Setting Description

A jumper pin-set is **ON** as a shorted circuit with a plastic cap inserted over two pins. A jumper pin-set is **OFF** as a open circuit with a plastic cap inserted over one or no pin(s) between pins. The below figure 2.2 shows the examples of different jumper pin-set setting as **ON** or **OFF** in this manual.

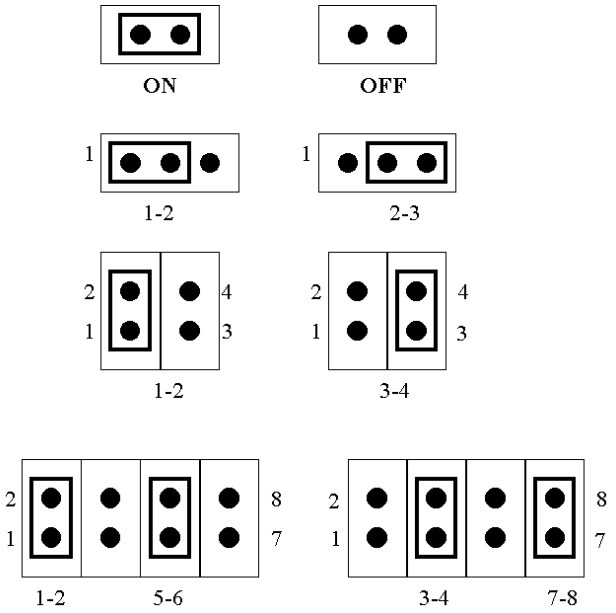


Figure 2.2

All jumper pin-set already has its default setting with the plastic cap inserted as ON, or without the plastic cap inserted as OFF. The default setting may reference in this manual with a " * " symbol in front of the selected item.

2.7 Setting the Bus-Clock Frequency

The TL-SBC 6620 provides all necessary by jumper setting in using Bus-Clock frequency as the system bus clocking with JP2 setting as following:

- **Bus-Clock Frequency Setting of JP2:**

Bus-Clock Frequency	JP2
*** 100MHz**	**OFF**
66MHz	ON

2.8 Frequency Multiplier Setting

The TL-SBC 6620 provides JP5 for define the selection of the Frequency Multiplier value of system bus to processor core in following table:

- **Frequency Multiplier Setting of JP5:**

Frequency Multiplier:					System Clock	
System Bus to Processor Core	7-8	5-6	3-4	1-2	JP5 ON	JP5 OFF
					66	* 100
3x	ON	ON	OFF	ON	200	300
4x	ON	ON	ON	OFF	266	400
5x	ON	ON	OFF	OFF	333	500
2.5x	ON	OFF	ON	ON	166	250
*** 3.5x**	**ON**	**OFF**	**OFF**	**ON**	**233**	*** 350**
4.5x	ON	OFF	ON	OFF	300	450
5.5x	OFF	ON	OFF	OFF	366	550
6x	ON	OFF	ON	ON	400	600
6.5x	OFF	OFF	ON	ON	430	650
7x	ON	OFF	OFF	ON	460	700
7.5x	OFF	OFF	OFF	ON	500	750
8x	ON	OFF	ON	OFF	530	800

The bus-clock is setting by JP2 and JP5 The default setting is for Intel Pentium®II 350MHz processor. If the bus Frequency not match processor frequency, the system will be unstable.

2.9 System Memory DRAM

The TL-SBC 6620 provides a wide range on-board DRAM memory by two pieces DIMM sockets (DIMM-1, DIMM-2) request the access time should meet PC-100 standard.. The maximum capacity of the on board memory is 1.0GBytes.

See the figure on section 2.3 for get the identifying the banks.

2.10 ATX/AT Power Select

The TL-SBC 6620 provides a selection by a three-pin jumper JP6 for setting the power supply type in using.

- **ATX/AT Power Select Setting of JP6:**

Power Supply In Using	JP6
ATX Power Supply	2-3
AT Power Supply	*** 1-2**

2.11 Watch-Dog Timer

There are three access cycles of Watch-Dog Timer as Enable, Refresh and Disable. The Enable cycle should proceed by READ PORT 443H. The Disable cycle should proceed by READ PORT 045H. A continue Enable cycle after a first Enable cycle means Refresh.

Once if the Enable cycle activity, a Refresh cycle is request before the time-out period for restart counting the WDT Timer's period. Otherwise, it will assume that the program operation is abnormal when the time counting over the period preset of WDT Timer. A System Reset signal to start again or a NMI cycle to the CPU comes if over.

The JP14 is using for select the active function of watch-dog timer in disable the watch-dog timer, or presetting the watch-dog timer activity at the reset trigger, or presetting the watch-dog timer activity at the NMI trigger.

- **JP14 : Watch-Dog Active Type Setting**

JP14	DESCRIPTION
***2-3**	**System Reset**
1-2	Active NMI
OFF	disable Watch-dog timer

- **JP10 (pin 5-6, 7-8, 9-10) : WDT Time - Out Period**

PERIOD	WD2	WD1	WD0
	5 – 6	7 – 8	9 – 10
***1 sec**	**ON**	**ON**	**ON**
2 sec	OFF	ON	ON
10 sec	ON	OFF	ON
20 sec	OFF	OFF	ON
110 sec	ON	ON	OFF
220 sec	OFF	ON	OFF

The Watch-dog timer is disabled after the system Power-On. The watch-dog timer can be enabled by a Enable cycle with reading the control port (443H), a Refresh cycle with reading the control port (443H) and a Disable cycle by reading the Watch-dog timer disable control port (045H). After a Enable cycle of WDT, user must constantly proceed a Refresh cycle to WDT before its period setting comes ending of every 1, 2, 16 or 256 seconds which pre-setting by JP10 (PIN 5-6, 7-8). If the Refresh cycle does not active before WDT period cycle, the on board WDT architecture will issue a Reset or NMI cycle to the system.

The Watch-Dog Timer is controlled by two I/O ports.

443H	I/O Read	The Enable cycle.
443H	I/O Read	The Refresh cycle.
045H	I/O Read	The Disable cycle.

The following sample programs showing how to Enable, Disable and Refresh the Watch-dog timer:

```
WDT_EN_RF       EQU     0443H
WDT_DIS         EQU     0045H
WT_Enable       PUSH    AX              ; keep AX DX
                PUSH    DX
                MOV     DX,WDT_EN_RF    ; enable the watch-dog
timer
                IN      AL,DX
                POP     DX              ; get back AX, DX
                POP     AX
                RET
WT_Rresh        PUSH    AX              ; keep AX, DX
                PUSH    DX
                MOV     DX,WDT_ET_RF    ; refresh the watch-dog
timer
                IN      AL,DX
                POP     DX              ; get back AX, DX
                POP     AX
                RET
WT_DISABLE      PUSH    AX
                PUSH    DX
                MOV     DX,WDT_DIS      ; disable the watch-dog
timer
                IN      AL,DX
```

```
POP     DX                  ; get back AX, DX
POP     AX
RET
```

2.12 PCI VGA Controller

The TL-SBC 6620 has built-in a C&T 69000 VGA Controller with on-chip 2 MB memory, support resolutions up to 1280 x 1024 256 colors to VGA-CRT monitor. The TL-SBC 6620 also provides one 50-pin internal LCD Panel connector CN10, and reserved internal 10-pin VGA-CRT header connector.

2.13 DiskOnChip™ Address Setting

The TL-SBC 6620 provides a U24 socket for install the DiskOnChip™ module.

A JP10 (pin 1-2, 3-4) may select the starting memory address of the DiskOnChip™ (D.O.C.) for avoid the mapping area with any other memory devices. If you have another extra memory devices in the system with the same memory, neither the TL-SBC 6620 nor the extra memory devices will function normally. Please setting both at different memory address mapping.

- **JP10 : DiskOnChip™ Address**

Memory Address Mapping	JP10 3-4	JP10 1-2
D000	*** ON**	*** ON**
D800	ON	OFF
E000	OFF	ON
E800	OFF	OFF

*) : default setting

The D.O.C. function allows the system in using without FDD nor HDD. The D.O.C. may formatting as driver C: or driver A:. User may also easily uses the DOS's commands such as FORMAT, SYS, COPY, XCOPY, DISCOPY and DISKCOMP etc. This is means that the D.O.C. may uses as driver-A if the system without FDD-A for ambient application. Please contact with your supplier for different size D.O.C. module.

2.14 LCD 3.3/5.0v Power Select

The TL-SBC 6620 provides a select for unsing the LCD Panel with 3.3V or 5.0V as setting in the following:

- **LCD Power Select of JP4:**

LCD Power Type	JP4
5.0V	*** 2-3**
3.3V	1-2

2.15 Manufacturer's Default Setting

The TL-SBC 6620 has some jumpers which are for design use only. Please set as the board provides of the manufacturer's default setting in the following:

- **Manufacturer's Default Setting of JP3 :**

Manufacturer's	Setting
JP3	*** OFF**

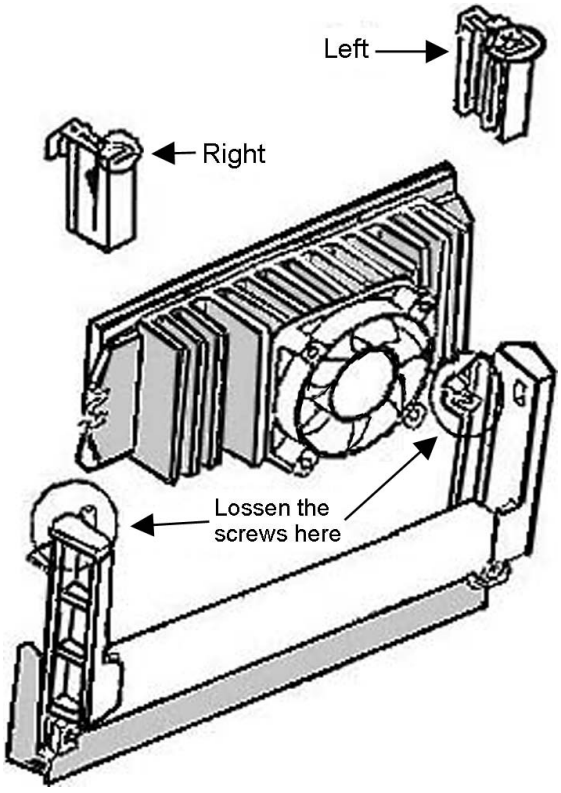
2.16 Temperature Alarm

The TL-SBC 6620 provides a select for Hardware temperature Alarm. If the CPU's temperature reached 60°C±10%, the warning "beep" will be come out. And it will stop as the CPU's temperature going down below 60°C±10% again.

- **Temperature Alarm Default Setting of JP7:**

Temperature Alarm	JP7
Enabled	**ON**
Disabled	**OFF**

2.17 Retention Mechanism



For SECC2 PII/III processor types, use the two caps on both ends after installing the processor to secure the installation. SECC types do not require these caps.

Chapter-3

Connection

This chapter gives all necessary information of the peripheral's connections, switches and indicators.

3.1 Power and FAN Connectors

The TL-SBC 6620 provides one 4-pin DC-Power connector as following CN7 pin information. And also provides one 3-pin fan out connector at solder side as following CN4 pin information.

- **CN7 : 4-PIN POWER CONNECTOR**

PIN NO.	DESCRIPTION
1	Vcc
2	GND
3	GND
4	+12V

- **CN4 : 3-PIN FAN IN/OUT CONNECTOR**

PIN NO.	Type	DESCRIPTION
1	To FAN	GND
2	To FAN	+12V
3	NC	NC

The output pin-2 (+12V) is a DC power to FAN.

3.2 IDE's LED, Key-Lock and Reset Button

The TL-SBC 6620 has one LED (D4) indicates out power-on status. And the following provides the pin information for IDE's LED connector, Key-Lock and Reset Button connections from CN3, CN1 and JP1.

- **CN3 : IDE LED connector**

PIN NO.	DESCRIPTION
1	HDD ACTIVE#
2	+5V

- **CN1 : POWER LED & KEYLOCK**

PIN NO.	DESCRIPTION
1	POWER LED ANODE
2	NC
3	GROUND
4	KEYLOCK
5	GROUND

- **JP1 : RESET BUTTON**

PIN NO.	DESCRIPTION
1	GROUND
2	EXTERNAL RESET

3.3 Extra Speaker Connector

The TL-SBC 6620 has an on-board buzzer (BZ1). And it also provides the CN2 in allows user to connecting to the external speaker.

- **CN2 : Speaker Connector**

PIN NO.	DESCRIPTION
1	SPEAKER SIGNAL
2	NC
3	GROUND

4	+5V

3.4 PCI E-IDE Drive Connector

Two standard 40-pin header daisy-chain driver connectors provide as CN8 and CN9 with following pin assignment. Total four IDE (Integrated Device Electronics) drivers may connect.

CN8 (IDE 1) : Primary IDE Connector

- **CN8 : IDE Interface Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	N/C	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	N/C	28	BALE - DEFAULT
29	N/C	30	GROUND# -DEFAULT
31	INTERRUPT	32	IOCS16#-DEFAULT
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0	38	HDC CS1#
39	HDD ACTIVE	40	GROUND

CN9 (IDE 2) : Secondary IDE Connector

- **CN9 : IDE Interface Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	N/C	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	N/C	28	BALE - DEFAULT
29	N/C	30	GROUND# -DEFAULT
31	INTERRUPT	32	IOCS16#-DEFAULT
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0	38	HDC CS1#
39	HDD ACTIVE	40	GROUND

3.5 PS/2 Power ON/OFF Control

The TL-SBC 6620 reserved a CN5 for ATX Power ON/OFF Control.

- **CN5 : ATX Power ON/OFF Control**

CN5	DESCRIPTION	
2	Pin 1-2 OFF (LOW)	Pin 1-2 ON (HIGH)
	Remain Power Status	Change Power ON / OFF
1	Standby 3.3V	

3.6 Parallel Port Connector

A standard 26-pin flat cable driver connector provides as CN12 with following pin assignment for connection to parallel printer.

- **CN12 : Parallel Port Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED
15	ERROR#	16	INITIINTELZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	GROUND

3.7 The Floppy Disk Drive Connector

A standard 34-pin header daisy-chain driver connector provides as CN16 with following pin assignment. Total two FDD drivers may connect.

- **CN16 : FDD CONNECTOR**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE DATA#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	GROUND	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT
33	GROUND	34	DISK CHANGE#

3.8 Serial Ports Connectors

- COM-1 RS-232 at external connector CN23.
- COM-1 RS-232 also at internal connector CN17.
- COM-2 RS-232 also at internal connector CN18.
- COM-2 RS-422/485 at internal connector CN13.

All COM ports provides with high speeds NS16C550 compatible UARTs with Read/Receive 16 byte FIFO serial ports. Please see the following pin assignment.

- **CN23/26 : RS-232 Serial Port DB-9 Connector (COM1/COM2)**

PIN NO.	DESCRIPTION
1	DATA CARRIER DETECT (DCD)
2	RECEIVE DATA (RXD)
3	TRANSMIT DATA (TXD)
4	DATA TERMINAL READY (DTR)
5	GROUND (GND)
6	DATA SET READY (DSR)
7	REQUEST TO SEND (RTS)
8	CLEAR TO SEND (CTS)
9	RING INDICATOR (RI)

- **CN17/18 : RS-232 Serial Port 10-pin Header (COM1/COM2)**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	RXD	4	RTX
5	TXD	6	CTX
7	DTR	8	RI
9	GND	10	NC

- **CN13 : RS422/485**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TX-	2	TX+
3	RX+	4	RX-
5	GND	6	RTS-
7	RTS+	8	CTS+
9	CTS-	10	NC

The table here in show out on how to select and setting the COM-2 as RS-232 as CN26 or CN18, or RS-422/485 at CN13.

Jumper	RS-232	RS-422/485
JP11	3-5, 4-6	1-3, 2-4
JP12	3-5, 4-6	1-3, 2-4
JP8	OPEN	3-4 or 1-2
JP9	OPEN	3-4 or 5-6

- **JP8 : Receiver Enable Control**

JP9	DESCRIPTION
1-2 ON	Always Enable
3-4 ON	Enable by writing the REG : 2 EFH BIT1=1
***1-2 OFF**	**Always Disable**

- **JP9 : Transceiver Enable Control**

JP9	DESCRIPTION
1-2 ON	Always Enable
3-4 ON	Enable by ”-RTS” signal
5-6 ON	Enable by writing the REG : 2 EFH BIT0=1
***1-2 OFF**	**Always Disable**

3.9 Keyboard Connectors

The TL-SBC 6620 offers two possibilities for keyboard connections to external PS/2 type keyboard at CN27 and an internal 5-pin header at CN6.

- **CN6 : 5-pin Header Keyboard Connector**

PIN NO.	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	N/C
4	GROUND
5	+5V

- **CN27 : 6-pin Mini-DIN Keyboard Connector**

PIN NO.	DESCRIPTION
1	KEYBOARD DATA
2	N/C
3	GROUND
4	+5V
5	KEYBOARD CLOCK
6	N/C

3.10 PS/2 Mouse 6-pin Mini-DIN Connector

The TL-SBC 6620 provides an external PS/2 mouse connector at CN24 with following pin information.

- **CN24 : PS/2 Mouse Connector**

PIN NO.	DESCRIPTION
1	DATA
2	NC
3	GROUND
4	+5V
5	CLK
6	NC

3.11 VGA-CRT Connector

The TL-SBC 6620 provides two possible connectives of VGA-CRT connections. One standard DB-15 external VGA connector as following CN25 pin information. Another internal 10-pin header for VRA-CRT connection as following CN19 pin information.

- **CN25 : 15-pin DB-15 Female VGA-CRT connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GROUND	6	GROUND
7	GROUND	8	GROUND
9	NC	10	GROUND
11	NC	12	NC
13	HSYNC	14	VSYNC
15	NC		

- **CN19 : 10-pin 5x2 Header VGA-CRT connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	2	GROUND
3	GREEN	4	GROUND
5	BLUE	6	GROUND
7	HSYNC	8	GROUND
9	VSYNC	10	GROUND

3.12 Flat-Panel Connector

The TL-SBC 6620 provides a 50-pin 2.0 mm pitch header connector (CN10) for 3.3Vor 5V Panel connection with following pin-assignment.

+12V	1	2	+12V
GND	3	4	GND
* +3.3 or +5V PVcc	5	6	ENAVdd
FPVee	7	8	GND
P_0	9	10	P_1
P_2	11	12	P_3
P_4	13	14	P_5
P_6	15	16	P_7
P_8	17	18	P_9
P_{10}	19	20	P_{11}
P_{12}	21	22	P_{13}
P_{14}	23	24	P_{15}
P_{16}	25	26	P_{17}
P_{18}	27	28	P_{19}
P_{20}	29	30	P_{21}
P_{22}	31	32	P_{23}
P_{24}	33	34	P_{25}
SHFCLK	35	36	FLM
M	37	38	LP
GND	39	40	ENABKL
P26	41	42	P27
P28	43	44	P29
P30	45	46	P31
P32	47	48	P33
P34	49	50	P35

*PVcc default +5V

Flat Panel Display interface

HS-XXXX		Mono	Mono	Mono	Color	Color	Color	Color	Color	Color	Color	Color	Color	Color
		SS	DD	DD	TFT	**TFT**	TFT	TFT	STN-HR	STN-SS	STN-SS	STN-DD	STN-DD	STN-DD
PIN #	Pin Name	8-bit	8-bit	16-bit	9/12/16 bit	**18 bit**	18/24 bit	36-bit	18/24 bit	8-bit (4bP)	16-bit (4bP)	8-bit (4bP)	16-bit (4bP)	24-bit
9	P0	D0	UD3	UD7	B0		B0	FB0	FB0	R1	R1	UR1	UR0	UR0
10	P1	D1	UD2	UD6	B1		B1	FB1	FB1	B1	G1	UG1	UG0	UG0
11	P2	D2	UD1	UD5	B2	**B0**	B2	FB2	FB2	G2	B1	UB1	UB0	UB0
12	P3	D3	UD0	UD4	B3	**B1**	B3	FB3	FB3	R3	R2	UR2	UR1	LR0
13	P4	D4	UD3	UD3	B4	**B2**	B4	FB4	SB0	B3	G2	LR1	UR0	LG0
14	P5	D5	UD2	UD2	G0	**B3**	B5	FB5	SB1	G4	B2	LG1	LG0	LB0
15	P6	D6	UD1	UD1	G1	**B4**	B6	SB0	SB2	R5	R3	LB1	LB0	UR1
16	P7	D7	UD0	UD0	G2	**B5**	B7	SB1	SB3	B5	G3	LR2	LR1	UG1
17	P8			UD7	G3		G0	SB2	FG0		B3		UG1	UB1
18	P9			UD6	G4		G1	SB3	FG1		R4		UB1	LR1
19	P10			UD5	G5	**G0**	G2	SB4	FG2		G4		UR2	LG1
20	P11			UD4	R0	**G1**	G3	SB5	FG3		B4		UG2	LB1
21	P12			UD3	R1	**G2**	G4	FG0	SG0		R5		LG1	UR2
22	P13			UD2	R2	**G3**	G5	FG1	SG1		G5		LB1	UG2
23	P14			UD1	R3	**G4**	G6	FG2	SG2		B5		LR2	UB2
24	P15			UD0	R4	**G5**	G7	FG3	SG3		R6		LG2	LR2
25	P16						R0	FG4	FR0					LG2
26	P17						R1	FG5	FR1					LB2
27	P18					**R0**	R2	SG0	FR2					UR3
28	P19					**R1**	R3	SG1	FR3					UG3
29	P20					**R2**	R4	SG2	SR0					UB3
30	P21					**R3**	R5	SG3	SR1					UR3
31	P22					**R4**	R6	SG4	SR2					LG3
32	P23					**R5**	R7	SG5	SR3					LB3
33	P24							FR0						
34	P25							FR1						
41	P26							FR2						
42	P27							FR3						
43	P28							FR4						
44	P29							FR5						
45	P30							SR0						
46	P31							SR1						
47	P32							SR2						
48	P33							SR3						
49	P34							SR4						
50	P35							SR5						
35	**SHFCLK:** Pixel clock .Shift Clock													
36	**FLM.VSYNC:** First line marker													
37	**DE,M:** Panel AC driver control													
38	**LP,HSYNC:** Latch pulse													
40	**ENABKL:** Power sequencing control for enabling the backlight.(high active)													

3.13 IR Connector

The TL-SBC 6620 provides a 6-pin internal IR communication connector as following CN21 pin information.

- **CN21 : 6-PIN IR CONNECTOR**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Vcc	4	GROUND
2	FIRRX	5	IRTX
3	IRRX	6	CVROFF

3.14 USB Port Connector

The TL-SBC 6620 provides a internal 8-pin header for two USB ports connection. Please refer to the following detail pin information.

- **CN20 : 8-pin Header USB Connector**

PIN NO.	CN20	PIN NO.	CN20
1	Vcc	2	Vcc
3	BD0-	4	BD1-
5	BD0+	6	BD1+
7	GROUND	8	GROUND

3.15 PC/104 Bus Connection

The TL-SBC 6620's PC/104 expansion bus provides you in connect to all kind of PC/104 modules. The PC/104 bus has been already become the industrial embedded 16-bit PC standard bus. You can easily install to over thousands type of PC/104 modules from hundreds of venders in the world. The detailed pin assignment of the PC/104 expansion bus connectors CN14 and CN15 are specified as following tables:

Note : The PC/104 connector allows to directly plug-in Stack-thru PC/104 modules without the PC/104 mounting kit.

- **CN14&CN15 : PC/104 Expansion Bus**
  (CN14 = 64-pin female connector; CN15 = 40-pin female connector.)

Pin No.	CN14 RowA	CN14 RowB	CN15 RowC	CN15 RowD
0	--	--	0V	0V
1	IOCHECK*	0V	SBHE*	MEMCS16*
2	SD7	RESETDRV	LA23	IOSC16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	NOWS*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	(KEY)	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	0V
19	SA12	REFRESH*	(KEY)	0V
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	DACK2*	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC	--	--
31	SA0	0V	--	--
32	0V	0V	--	--

3.16 Fast Ethernet Connector

The Fast Ethernet controller provides with 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3 10/100Based-T specifications.

For 10/100Base-T operation, please connect the network connection by plugging one end of the cable into the 9-pin RJ-45 CN22 Connector.

- **CN22 : Ethernet Connector (9-pin RJ-45)**

PIN NO.	DESCRIPTION
1	TX+
2	TX-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC
9	Ground

For indication out the LAN operating status, the board provides three LED indicators in show out the status at follows:

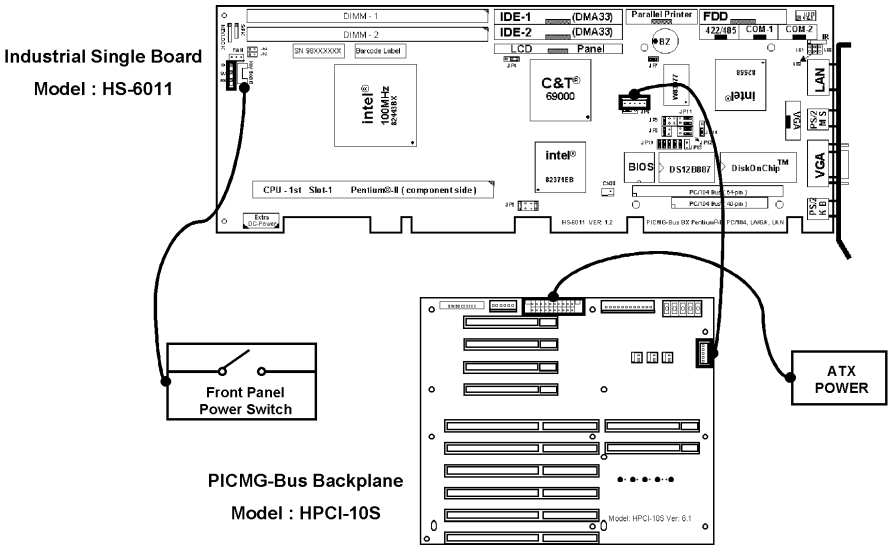
LE1: LED indicator lighting shows 10-Based data rating

LE2: LED indicator lighting shows 100-Based data rating

LE4: LED indicator lighting shows LAN in active

3.17 ATX Power Controller Connector

The TL-SBC 6620 support ATX Power function by CN11. The connector of CN11 can control the 5 pin ATX Power via the extension cable from the Backplane (from the version 6.1).



Chapter-4

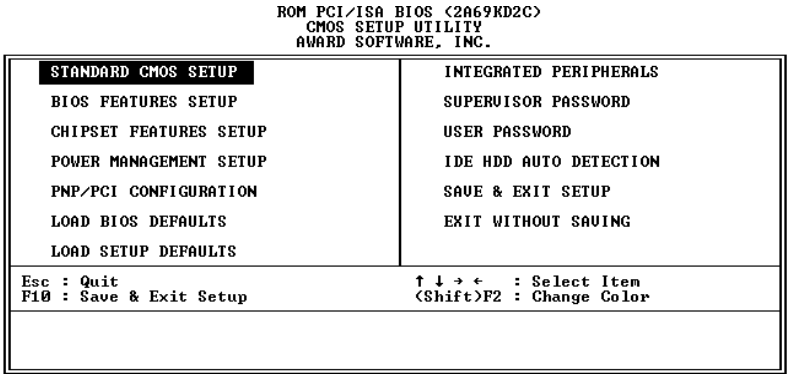
AWARD BIOS Setup

The TL-SBC 6620 uses the Award PCI/ISA BIOS for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press <Del> key. The Main Menu will be displayed at this time.

4.1 Main Menu

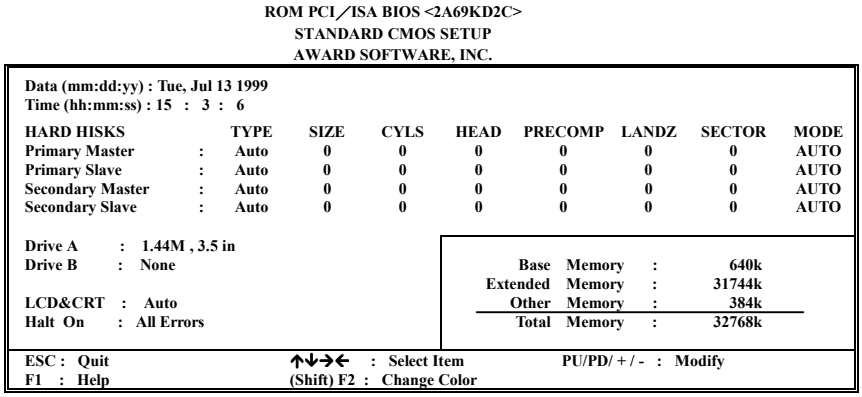
Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to enter the sub-menu.



Note that a brief description of each highlighted selection appears at the bottom of the screen.

4.2 Standard CMOS Setup

The Standard Setup is used for the basic hardware system configuration. The main function is for Data/Time and Floppy/Hard Disk Drive settings. Please refer to the following screen for the setup. When the IDE hard disk drive you are using is larger than 528MB, please set the HDD mode to **LBA** mode. Please use the IDE Setup Utility in BIOS SETUP to install the HDD correctly.


ROM PCI／ISA BIOS <2A69KD2C>
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.
Data (mm:dd:yy) : Tue, Jul 13 1999
Time (hh:mm:ss) : 15 : 3 : 6
HARD HISKS TYPE SIZE CYLS HEAD PRECOMP LANDZ SECTOR MODE
Primary Master : Auto 0 0 0 0 0 0 AUTO
Primary Slave : Auto 0 0 0 0 0 0 AUTO
Secondary Master : Auto 0 0 0 0 0 0 AUTO
Secondary Slave : Auto 0 0 0 0 0 0 AUTO
Drive A : 1.44M , 3.5 in
Drive B : None
LCD&CRT : Auto
Halt On : All Errors
Base Memory : 640k
Extended Memory : 31744k
Other Memory : 384k
Total Memory : 32768k
ESC : Quit
F1 : Help
↑↓→← : Select Item
(Shift) F2 : Change Color
PU/PD/ + / - : Modify

4.3 BIOS Features Setup

This section allows you to configure your system for the basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

ROM PCI／ISA BIOS <2A69KD2C>
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS	Shadow	: Enabled	
CPU Internal Cache	: Enabled	C8000-CBFFF	Shadow	: Disabled	
External Cache	: Enabled	CC000-CFFF	Shadow	: Disabled	
CPU L2 Cache ECC Checking	: Enabled	D0000-D3FFF	Shadow	: Disabled	
Quick Power On Self Test	: Disabled	D4000-D7FFF	Shadow	: Disabled	
Boot Sequence	: A,C,SCSI	D8000-DBFFF	Shadow	: Disabled	
Swap Floppy Drive	: Disabled	DC000-DFFFF	Shadow	: Disabled	
Boot Up Floppy Seek	: Enabled				
Boot Up NumLock Status	: On				
Gate A20 Option	: Fast				
Typematic Rate Setting	: Disabled				
Typematic Rate (Chars/Sec)	: 6				
Typematic Delay (Msec)	: 250				
Security Option	: Setup				
PS/2 mouse function conltrol	: Enabled				
PCI/VGA Palette Snoop	: Disabled	ESC : Quit		↑↓→←: Select Item	
OS Select For DRAM > 64MB	: Non-OS2	F1 : Help		PU / PD / + /- : Modify	
Report No FDD For WIN 95	: Yes	F5 : Old Values		(Shift) F2 : Color	
		G6 : Load BIOS Defaults			
		G7 : Load Setup Defaults			

4.4 Chipset Features Setup

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and the access to the system memory resources, such as DRAM and the external cache. It also coordinates the communications between the conventional ISA and PCI buses. It must be stated that these items should never be altered. The default settings have been chosen because they provide the best operating conditions for your system. You might consider and make any changes only if you discover that the data has been lost while using your system.

ROM PCI／ISA BIOS <2A69KD2C>
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	:	Enabled	Auto Detect DIMM/PCI Clk	:	Enabled
EDO DRAM Speed Selection	:	60ns	Spread Spectrum	:	Disabled
EDO CASx# MA Wait State	:	2	CPU Host Clock	:	Default
EDO RASx# Wait State	:	2	CPU Warning Temperature	:	Disabled
SDRAM RAS-to-CAS Delay	:	3	Current CPU Temperature	:	35°C / 95°F
SDRAM RAS Precharge Time	:	3			
SDRAM CAS latency Time	:	3			
SDRAM Precharge Control	:	Disabled			
DRAM Date Integrity Mode	:	Non-ECC			
System BIOS Cacheable	:	Enabled			
Video BIOS Cacheable	:	Enabled			
Video RAM Cacheable	:	Enabled			
8 Bit I/O Recovery	:	1			
16 Bit I/O Recovery	:	1			
Memory Hole At 15M-16M	:	Disabled			
Passive Release	:	Disabled	ESC : Quit	↑↓→←: Select Item	
Delayed Transation	:	Enabled	F1 : Help	PU/PD/+/- : Modify	
AGP Aperture Size	:	64	F5 : Old Values	(Shift) F2 : Color	
			F6 : Load BIOS Defaults		
			F7 : Load Setup Defaults		

4.5 Integrated Peripherals

The IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship which is determined by the cabling configuration used to attach them to the controller. Your system supports two IDE controllers--a primary and a secondary--so you can install up to four separate hard disks.

PIO means Programmed Input /Output. Rather than having the BIOS issue a series of commands to affect the transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by them. This is much simpler and more efficient (also faster).

ROM PCI／ISA BIOS <2A69KD2C>
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC.

IDE HDD Block Mode	: Enabled		
IDE Primary Master PIO	: Auto	Onboard Parallel Port	: 378 / IRQ7
IDE Primary Slave PIO	: Auto	Parallel Port Mode	: SPP
IDE Primary Master PIO	: Auto		
IDE Primary Slave PIO	: Auto		
IDE Primary Master UDMA	: Auto		
IDE Primary Slave UDMA	: Auto		
IDE Primary Master UDMA	: Auto		
IDE Primary Slave UDMA	: Auto		
On-Chip Primary PCI IDE	: Enabled	LCD Panel Type	: Panel 5
On-Chip Secondary PCI IDE	: Enabled		
USB Keyboard Support	: Disabled		
Init Display First	: PCI Slot		
KBC input clock	: 8MHz		
Onboard FDC Controller	: Enabled	ESC : Quit	↑↓→← : Select Item
Onboard Serial Port 1	: 3F8/IRQ4	F1 : Help	PU/PD/+/- : Modify
Onboard Serial Port 2	: 2F8/IRQ3	F5 : Old Values	(Shift) F2 : Color
UART Mode Select	: Normal	F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

4.6 Power Management Setup

The Power Management Setup allows user to configure the system for saving energy in a most effective way while operating in a manner consistent with his own style of computer use.

ROM PCI-ISA BIOS <2A69KD2C>
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	:	User Define	** Reload Global Timer Events **		
PM Control by APM	:	Yes	IRQ3 [3-7, 9-15], NMI	:	Disabled
Video Off Method	:	V/H SYNC + Blank	Primary IDE0	:	Disabled
Video Off After	:	Standby	Primary IDE1	:	Disabled
MODEM Use IRQ	:	3	Secondary IDE 0	:	Disabled
Doze Mode	:	Disable	Secondary IDE 1	:	Disabled
Standby Mode	:	Disable	Floppy Disk	:	Disabled
Suspend Mode	:	Disable	Serial Port	:	Enabled
HDD Power Down	:	Disable	Parallel Port	:	Disabled
Throttle Duty Cycle	:	62.5%			
PCI/VGA Act-Monitor	:	Disabled			
Power On by Ring	:	Instant-Off			
CPU fan on temp high	:	Enabled			
IRQ8 Break Suspend	:	Disabled			
			ESC : Quit	↑↓→← :	Select Item
			F1 : Help	PU/PD/+/- :	Modify
			F5 : Old Values	(Shift) F2 :	Color
			F6 : Load BIOS Defaults		
			F7 : Load Setup Defaults		